Constraint driven design using OrCAD® PCB design tools
About the author

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  – Master in Electronics Engineering
  – 14+ years in EDA industry working with and serving the Danish industry.
  – www.nordcad.dk

• Work tasks
  – Hotline support, training and services for Cadence software in Denmark
  – Startup service to companies adopting Cadence tools.
  – Great experience in building a solid constraint driven hw development flow
  – Skill programming
  – Danish technical newsletter e-SERVICE with tips and tricks, movies etc.
  – Presentation and demonstration of EDA software from Cadence.
Agenda

• Introduction
• Control constraints using Cadence® OrCAD® PCB Design tools
  – Flow
  – Basic principle & goal
  – Constraint overview
  – From Capture to PCB Editor
  – Build constraint template
    – Example
  – User your constraint template
  – Constraint matchup principle
  – Finalizing the PCB
• Wrapup
• Appendices
  – Identify critical nets
  – Constraint Hierarchy
• Q&A

• What is a constraint driven flow?
  – Automated communication of design intent
Are you confused ????

- Passing constraints
  - Plenty information channels
  - Lots of information
  - Many sources
  - Is the information contradicting
  - Is the design "over constrained"

- Could there be a reason if the result is far from optimum?
Make it simple and efficient!

- Communication – made simple and efficient
- Let’s talk the same “language”

- What You Communicate Is What You Get (WYCIWYG)
Optimize the flow

- Standardize constraint communication
  - Build constraint standards
  - Pass constraints from Schematic to PCB
  - Specify constraints early in the design process

- Review functionality
  - Cross-probing
  - Measure and review constraints
  - Reports
  - DRC check and design status
  - Extract to SI Analysis

PCB Design (Internal/External)

PCB Review with SI analysis and Crossprobing
Basic principle & goal

• GOAL:
  – Communicate constraints from OrCAD Capture to OrCAD PCB Editor
  – Reduce numerous communication sources to just a few or preferably one!

• Basic principle
  1. Create constraint template spreadsheet
  2. Create PCB template
  3. Communicate workflow and naming conventions to all in design team
  4. Use naming conventions in Capture
  5. Import schematic to PCB Editor
  6. PCB designer refines constraints for specific job if needed
  7. Place and route
  8. Review PCB
  9. Postprocess

Involve relevant people in building this flow, could be
  • Front-end designers
  • PCB designers
  • PCB manufacturer
  • Production
  • Etc.
Constraint overview

• All constraints are controlled using Constraint Manager in PCB Editor
  – Physical
    – Line width, via types, routing layers
  – Spacing (and same-net-spacing)
    – Line to line, via to line, pin to via etc.
  – Electrical (available in Allegro PCB Design Performance Option and higher)
    – Matched length, differential pairs etc.

• Constraint Sets (CSets) – what are they
  – Collection of constraints (e.g., width, via type, layers)
    • Default: 0.2mm width, via60h25, route on all layers
    • 50ohm: 0.32mm on outer layers, 0.3mm on inner layers
  – Comparable to Microsoft Word styles
    • Heading 1: Arial 15, Bold, font color red
  – 3 types: Physical, Spacing and Electrical

– Nets and Netclasses can refer to a Constraint Set
  – Will inherit constraints from referred Cset
From Capture to PCB Editor

- Capture communicates with PCB Editor through a netlist
  - Components and component/function/pin properties
  - Nets and net properties
- Important net properties
  - ‘Net_physical_type’
    - property name added to net → Net is added to Physical Netclass
    - Physical Netclass can reference Physical Constraint Set (PCset)
  - ‘Net_spacing_type’
    - property name added to net → Net is added to Spacing Netclass
    - Spacing Netclass can reference Spacing Constraint Set (SCset)
  - ‘Electrical_constraint_set’
    - property name added to net → Net refers directly to Electrical Constraint Set (ECSet)

Notice: nets without
- Net_spacing_type
- Net_physical_type
- Electrical_constraint_set
uses default Constraint Set
Build your constraint template

- Create a spreadsheet with standard constraint specifications
  - Netclass names
  - Constraint set names and key constraint values
- Create an empty PCB design (template) with
  - Constraints sets: spacing, physical (and electrical)
  - Netclasses
- Create the necessary relations between netclasses and constraint sets
Example spreadsheets

Physical constraint setup

<table>
<thead>
<tr>
<th>Net_Physical_Type</th>
<th>Width</th>
<th>Via type</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;None&gt;</td>
<td>0.2mm</td>
<td>via26</td>
</tr>
<tr>
<td>Power</td>
<td>0.5mm</td>
<td>via40</td>
</tr>
<tr>
<td>AD</td>
<td>0.1mm</td>
<td>via26</td>
</tr>
</tbody>
</table>

Constraint Sets in PCB Editor

| 01mm   | 0.1mm | via26 |
| 02mm   | 0.2mm | via26 |
| 05mm   | 0.5mm | via40 |

Via names

<table>
<thead>
<tr>
<th>Size</th>
<th>Hole</th>
</tr>
</thead>
<tbody>
<tr>
<td>Via40</td>
<td>1mm</td>
</tr>
<tr>
<td>Via26</td>
<td>0.7mm</td>
</tr>
<tr>
<td>Via75</td>
<td>2mm</td>
</tr>
</tbody>
</table>

Spacing constraint setup

<table>
<thead>
<tr>
<th>Net_Spacing_Type</th>
<th>&lt;None&gt;</th>
<th>Power</th>
<th>AD</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;None&gt;</td>
<td>0.2mm</td>
<td>0.5mm</td>
<td>0.2mm</td>
</tr>
<tr>
<td>Power</td>
<td>0.5mm</td>
<td>0.5mm</td>
<td></td>
</tr>
<tr>
<td>AD</td>
<td></td>
<td>0.1mm</td>
<td></td>
</tr>
</tbody>
</table>

Constraint Sets in PCB Editor

<table>
<thead>
<tr>
<th>L-L</th>
<th>L-S</th>
<th>V-S</th>
<th>V-V</th>
<th>V-P</th>
</tr>
</thead>
<tbody>
<tr>
<td>01mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
</tr>
<tr>
<td>02mm</td>
<td>0.2mm</td>
<td>0.2mm</td>
<td>0.2mm</td>
<td>0.2mm</td>
</tr>
<tr>
<td>05mm</td>
<td>0.5mm</td>
<td>0.5mm</td>
<td>0.5mm</td>
<td>0.5mm</td>
</tr>
</tbody>
</table>

Legend

<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Line, Track/cline</td>
</tr>
<tr>
<td>P</td>
<td>Pin, Component pin</td>
</tr>
<tr>
<td>S</td>
<td>Shape, Copper pour/area</td>
</tr>
<tr>
<td>V</td>
<td>Via</td>
</tr>
</tbody>
</table>

Electrical constraint setup

<table>
<thead>
<tr>
<th>Electrical CSets</th>
<th>Constraints</th>
<th>Constraint</th>
</tr>
</thead>
<tbody>
<tr>
<td>50Ohm</td>
<td>Impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td>55Ohm</td>
<td>Impedance</td>
<td>55Ω</td>
</tr>
<tr>
<td>DDR2_Addr</td>
<td>Wiring</td>
<td>Topology</td>
</tr>
<tr>
<td></td>
<td>Impedance</td>
<td>50Ω</td>
</tr>
<tr>
<td></td>
<td>Matchgroup</td>
<td>Matched length</td>
</tr>
<tr>
<td>DDR2_CLK</td>
<td>Wiring</td>
<td>Topology</td>
</tr>
<tr>
<td></td>
<td>Diff impedance</td>
<td>100Ω</td>
</tr>
</tbody>
</table>

• These are just examples
  – Build to fit your needs!
• Communicate to schematic designers
  – They should use correct Netclass names
Use your constraint template

- Use the Netclass (net_spacing/physical_type) names inside OrCAD Capture
- Create a netlist and import into PCB template design
  - Nets with correct Netclass names are now automatically matched with constraint sets
    - Using PCB template constraints
- Keep updating the constraint template and spreadsheet to accommodate new requirements
Constraint matchup

Import netlist in template

Net_spacing_type?

No

Use default spacing constraints

Yes

Include net in predefined Spacing Netclass and use constraints assigned to this netclass

Net_physical_type?

No

Use default physical constraints

Yes

Include net in predefined Physical Netclass and use constraints assigned to this netclass

Electrical_constraint_set?

No

Do not assign ECSet

Yes

Assign net Electrical_constraint_set

Constraint matchup complete

Notice: nets without
- Net_spacing_type
- Net_physical_type
- Electrical_constraint_set uses default Constraint Set
Finalizing the PCB

- After constraint matchup
  - PCB Designer refines the constraints if necessary
  - Finish up the PCB (place, route etc.)
- Review using standard functionality
  - Cross-probing from Capture to PCB Editor to highlight elements
  - Display → Status (DRC update/check)
  - Display → Constraints
  - Extract to SigXplorer for SI analysis
What are the benefits

• Control the design flow
  – *Default constraints are part of the PCB template*
  – *Use of the correct names during schematic entry automates most of the constraint setup*
  – *The PCB Designer can concentrate on primary tasks since constraints are passed using a standardized methodology*
  – *Constraints can be reused and a library of verified constraints is built*
  – *Running Design Rule Check verifies the passed constraints*
  – *All designers talk the same language*
    – makes designing much easier
    – documentation is more consistent
    – Constraint review is easier and faster
  – *Less errors due to consistency throughout the flow – What You Communicate Is What You Get (WYCIWYG)*

• *Questions*
Appendices
Identify ’critical’ nets

- Identify critical nets (needs special constraints otherwise DEFAULT is used)
  - Specify NET_PHYSICAL_TYPE if special physical requirements
  - Specify NET_SPACING_TYPE if special spacing or same-net-spacing requirements
  - Specify ELECTRICAL_CONSTRAINT_SET if any Electrical constraint requirements
    - only Performance Option and higher

- Build tables with key information
  - Enhance as needed
  - You decide the level of details

<table>
<thead>
<tr>
<th>Class</th>
<th>Tech</th>
<th>Layers</th>
<th>Stub</th>
<th>Width</th>
<th>Spacing</th>
<th>Internal Spacing</th>
<th>Via</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diff</td>
<td>STL</td>
<td>Internal</td>
<td>3 mm</td>
<td>Outer: 0.9mm</td>
<td>0.4mm</td>
<td>0.2mm</td>
<td>0.25 mm hole &amp; BB Vias</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Inner: 0.85mm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data</td>
<td>STL</td>
<td>L2-3, L5-6, L8-9</td>
<td>4 mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.25 mm hole &amp; BB Vias</td>
</tr>
<tr>
<td>Address</td>
<td>STL</td>
<td>All</td>
<td>4 mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.1mm</td>
<td>0.25 mm hole &amp; BB Vias</td>
</tr>
<tr>
<td>Power</td>
<td>PWR</td>
<td>All</td>
<td></td>
<td>0.2mm</td>
<td>0.2mm</td>
<td>0.2mm</td>
<td>0.25 mm hole &amp; BB Vias</td>
</tr>
</tbody>
</table>

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